


[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) |

Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "((((data<or>clock)<near/3>recovery)<and>serdes)<in>metadata)"

☒ e-mail

Your search matched 14 of 1360403 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

[View Session History](#)[New Search](#)

Modify Search

((((data<or>clock)<near/3>recovery)<and>serdes)<in>metadata)

☐ Check to search only within this results setDisplay Format: ☒ Citation ☐ Citation & Abstract

» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

[Select All](#) [Deselect All](#)

- ☐ 1. A 40-43-Gb/s clock and data recovery IC with integrated SFI-5 1:16 demul technology
Ong, A.; Benyamin, S.; Cancio, J.; Conditto, V.; Labrie, T.; Qinghung Lee; Matti D.K.; Shahani, A.; Xiaomin Si; Hai Tao; Tarsia, M.; Wong, W.; Min Xu;
[Solid-State Circuits, IEEE Journal of](#)
Volume 38, Issue 12, Dec 2003 Page(s):2155 - 2168
Digital Object Identifier 10.1109/JSSC.2003.818565
[AbstractPlus](#) | Full Text: [PDF\(1583 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 2. Equalization and clock recovery for a 2.5-10-Gb/s 2-PAM/4-PAM backplan cell
Zerbe, J.L.; Werner, C.W.; Stojanovic, V.; Chen, F.; Wei, J.; Tsang, G.; Kim, D W.F.; Ho, A.; Thrush, T.P.; Kollipara, R.T.; Horowitz, M.A.; Donnelly, K.S.;
[Solid-State Circuits, IEEE Journal of](#)
Volume 38, Issue 12, Dec 2003 Page(s):2121 - 2130
Digital Object Identifier 10.1109/JSSC.2003.818572
[AbstractPlus](#) | Full Text: [PDF\(2168 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 3. A 10-GB/s SONET-compliant CMOS transceiver with low crosstalk and in Werker, H.; Mechnig, S.; Holuigue, C.; Ebner, C.; Mitteregger, G.; Romani, E.; T.; Moyal, M.; Vena, M.; Melodia, A.; Fisher, J.; de Mercay, G.L.G.; Geib, H.;
[Solid-State Circuits, IEEE Journal of](#)
Volume 39, Issue 12, Dec. 2004 Page(s):2349 - 2358
Digital Object Identifier 10.1109/JSSC.2004.835652
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(1536 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☒ 4. Clock and data recovery with adaptive loop gain for spread spectrum Ser Ming-ta Hsieh; Sobelman, G.E.;
[Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on](#)
23-26 May 2005 Page(s):4883 - 4886 Vol. 5
Digital Object Identifier 10.1109/ISCAS.2005.1465727
[AbstractPlus](#) | Full Text: [PDF\(296 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☒ 5. A low jitter, low power, CMOS 1.25-3.125Gbps transceiver